PATENT ABSTRACTS OF JAPAN

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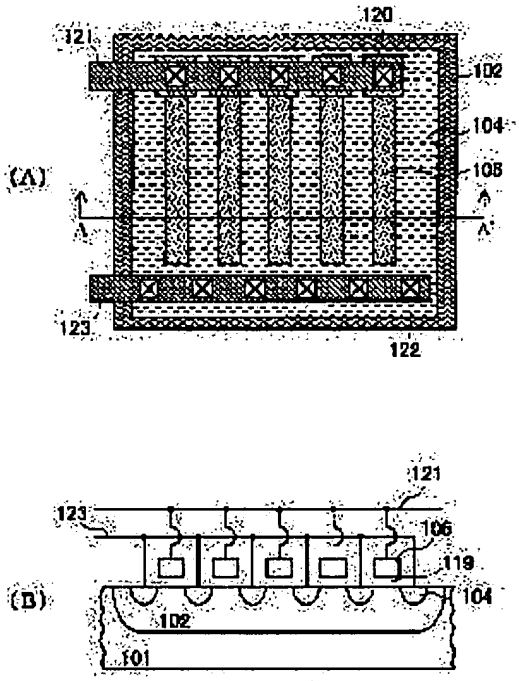
(54) VOLTAGE-GENERATING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To boost a voltage without increasing a chip area and without entailing a voltage step-up loss due to a back bias effect.
SOLUTION: A gate electrode 106 of a polysilicon film is formed like teeth of a comb by a minimum line width and a minimum distance regulated by a design rule via a gate oxide film 119 on an N type well 102 formed to a P type silicon substrate 101. An N type impurity region 104 is formed except below the gate electrode 106 to the well 102 in the periphery of the gate electrode 106. In this arrangement, influences of a parasitic resistance and a parasitic capacitance of the well 102 can be eliminated. Although an area where the well 102 faces the gate electrode 106 is made approximately half, a capacitance between end parts and side walls of the gate electrode 106, and the well 102 and a contact metal 120 increases and therefore a total capacitance hardly decreases.



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